CLAIM AMENDMENTS

1. (Previously Presented) A system comprising:

a locked loop circuit to indicate a timing between an input signal and an output signal; and

a processor coupled to the locked loop circuit to based on the indication of the timing control the locked loop circuit and perform at least one other function in the system not related to the control of the locked loop circuit.

2. (Original) The system of claim 1, wherein the locked loop circuit comprises a delay locked loop circuit.

3. (Original) The system of claim 1, wherein the locked loop circuit comprises:

an interface accessible by the processor.

4. (Previously Presented) The system of claim 3, wherein the interface indicates a phase difference between the input signal and the output signal.

5. (Original) The system of claim 3, wherein the system comprises a computer system having a system memory and the interface is addressable in a range of addresses used to access the system memory.

6. (Original) The system of claim 3, wherein the interface indicates storage accessible by the processor to store an indication of a delay used by the locked loop circuit.

7. (Original) The system of claim 3, wherein the interface includes storage accessible by the processor to store an indication of a selection of one or more of a plurality of output clock signals furnished by the locked loop circuit.

8. (Original) The system of claim 1, wherein the processor comprises a microprocessor.

9. (Original) The system of claim 1, further comprising:

a system memory storing a program,

wherein the processor executes the program to perform said other function.

10. (Currently Amended) A locked loop circuit comprising:

a delay line to introduce a delay to ~~receive~~ an input clock signal to produce ~~and furnish~~ an output clock signal;

a phase detector to indicate a phase difference between the input clock signal and the output clock signal; and

an interface accessible by a processor to regulate the delay ~~control the locked loop circuit~~ to adjust a timing between the input clock signal and the output clock signal based on the indicated phase difference.

11. (Original) The locked loop circuit of claim 10, wherein the locked loop circuit comprises a delay locked loop circuit.

12. (Original) The locked loop circuit of claim 10, wherein the interface indicates a phase difference between an incoming clock signal to the locked loop circuit and another signal generated by the locked loop circuit.

13. (Original) The locked loop circuit of claim 10, wherein the interface is addressable in a range of addresses used to access a system memory of a computer system.

14. (Currently Amended) The locked loop circuit of claim 10, wherein the interface includes storage accessible by the processor to store an indication of [[a]] the delay ~~applied by the locked loop circuit to the input clock signal~~.

15. (Original) The locked loop circuit of claim 10, wherein the interface includes storage accessible by the processor to store an indication of a selection of one of a plurality of output clock signals furnished by the locked loop circuit.

16. (Currently Amended) A method comprising:

providing a locked loop circuit having a processor accessible interface and indicating a timing between an input signal and an output signal of the locked loop circuit; and

using a processor to control a delay introduced by the locked loop circuit between the input and output signals based on the indicated timing and perform at least one other function not related to the control of the locked loop circuit.

17. (Original) The method of claim 16, wherein the locked loop circuit comprises a delay locked loop circuit.

18. (Original) The method of claim 16, further comprising:

performing at least one of read and write operations to the interface to control the locked loop circuit.

19. (Original) The method of claim 16, further comprising:

using the interface to indicate a phase difference between an input clock signal and an output clock signal generated by the locked loop circuit.

20. (Original) The method of claim 16, wherein the system comprises a computer system having a system memory and the interface is addressable in a range of addresses used to access the system memory.

21. (Original) The method of claim 16, further comprising:

using the interface to store an indication of a delay used by the locked loop circuit.

22. (Original) The method of claim 16, further comprising:

using the interface to store an indication of a selection of one or more of a plurality of output clock signals furnished by the locked loop circuit.

23. (Original) The method of claim 16, wherein the processor comprises a microprocessor.

24. (Currently Amended) An article comprising a computer accessible storage medium storing instructions to, when executed, cause a processor to:

receive an indication of a phase difference from a locked loop circuit and control a delay introduced by the locked loop circuit between an input signal and an output signal of the locked loop circuit based on the indicated phase difference, wherein the processor performs at least one other function not related to the control of the locked loop circuit.

25. (Previously Presented) The article of claim 23, wherein the locked loop circuit comprises a delay locked loop circuit.

26. (Previously Presented) The article of claim 24, the storage medium storing instructions to cause the processor to use an interface to receive the indication of the phase difference.

27. (Previously Presented) The article of claim 24, the storage medium storing instructions to cause the processor to store an indication of a delay used by the locked loop circuit in an interface of the locked loop circuit.

28. (Previously Presented) The article of claim 24, the storage medium storing instructions to access an interface of the locked loop circuit to store an indication of a selection of one or more of a plurality of output clock signals furnished by the locked loop circuit.

29. (New) The system of claim 1, wherein the delay locked loop circuit comprises a delay chain to establish a delay between the input signal and the output signal, and the processor controls the delay chain based on the indicated timing between the input signal and the output signal.